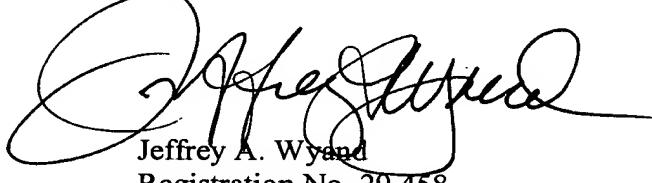


REMARKS

The foregoing Amendment corrects translational errors and conforms the claims to United States practice.

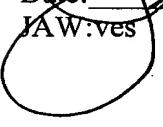
Respectfully submitted,

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PATENT
Attorney Docket No. 401265/FUKAMI

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

YOSHIHIKO TOYODA

Art Unit: Unknown

Application No.: Unknown

Examiner: Unknown

Filed: June 28, 2001

For: SEMICONDUCTOR
DEVICE AND
MANUFACTURING
METHOD THEREOF

**SPECIFICATION, CLAIMS AND
ABSTRACT AS PRELIMINARILY AMENDED**

Amendments to the paragraph beginning at page 1, line 31:

Referring to Fig. 41, the a thick Cu film 105 is thickly deposited on the entire surface by electrolytic plating in a plating liquid of a copper sulfate bath, ~~so as to be and~~ embedded in the respective grooves 102a, 102b. At this time, the depositing rate ~~becomes~~ is faster in narrow sections such as narrow grooves and holes 102b than in wide grooves 102a and flat face portions due to the effects of additives added in the plating liquid, ~~with the~~. As a result that, the embedding is preferentially carried out in these portions, and thus, it is possible to obtain a superior embedding property. Moreover, the Cu film 105 ~~formed in the portions except~~ deposited outside the grooves 102a, 102b is removed by a chemical mechanical polishing method (CMP method), thereby providing a the semiconductor device shown in Fig. 38

Amendments to the paragraph beginning at page 2, line 22:

In order to remove all the thick Cu film 105 on the narrow groove 102b by the CMP method, the thin Cu film 105 on the wide groove 102a needs to be excessively abraded. As a result, the upper surface of wires 104, 105 formed inside the wide groove 102a is ~~concaved~~ becomes concave. Consequently, there is a great increase in the

resistivity of the wire inside the wide groove 102a, or there are great deviations in the resistivity.

Amendments to existing claims:

1. (Amended) A semiconductor device comprising:
~~an insulating layer having a surface in which and including a plurality of grooves having different widths are formed; and~~
~~a conductive layer formed by filling the inside of each of said the grooves with and including at least plating a plated layer, wherein unevenness is formed on a bottom portion of each of some of the grooves among said plurality of grooves is non-planar.~~
2. (Amended) The semiconductor device according to claim 1, wherein ~~said unevenness is formed on a the non-planar bottom portion of a groove that has portions have a ratio of the depth to the width of not more than 0.7.~~
3. (Amended) The semiconductor device according to claim 1, wherein ~~said unevenness is formed on a the non-planar bottom portion of a groove that has portions have a ratio of the depth to the width of not more than 0.35.~~
4. (Amended) The semiconductor device according to claim 1, wherein the ~~non-planar bottom portions include a concave portion of said unevenness has having a groove shape, and said concave portion has with a ratio of the depth to the width of greater than 0.35.~~
5. (Amended) The semiconductor device according to claim 1, wherein the ~~non-planar bottom portions include a concave portion of said unevenness has having a groove shape, and said concave portion has with a ratio of the depth to the width of greater than 0.7.~~

6. (Amended) The semiconductor device according to claim 1, wherein the non-planar bottom portion includes a concave portion of said unevenness having a hole shape, and said concave portion has with a ratio of the depth to the width of greater than 0.35.

7. (Amended) The semiconductor device according to claim 1, wherein the non-planar bottom portion includes a concave portion of said unevenness having a hole shape, and said concave with a ratio of the depth to the width of greater than 0.7.

8. (Amended) The semiconductor device according to claim 1, wherein the non-planar bottom portion has a concave portion of said unevenness having two slanting side faces with the two side faces crossing intersecting each other in its cross-section a cross-sectional view.

9. (Amended) The semiconductor device according to claim 8, wherein the side face of said concave portion is faces are slanted with an angle greater than 20 degrees against an upper relative to the surface of said insulating layer.

10. (Amended) The semiconductor device according to claim 1, wherein the non-planar bottom portions of the grooves have concave portions with a pitch of said concave portions of said unevenness is set to be not more than 4 times the width or the aperture diameter of the concave portion portions.

11. (Amended) A manufacturing method of a semiconductor device comprising:
the steps of:

forming a plurality of grooves having different widths on a surface of an insulating layer, and forming unevenness on a non-planar bottom surface of each of surfaces in some grooves among said of the plurality of grooves;

~~depositing plating a metal film on said insulating layer by plating so as to be and embedded in said the plurality of grooves and said unevenness on the non-planar bottom portions; and~~

~~removing said metal film by chemical mechanical polishing until at least the upper surface of said insulating layer is exposed so that said metal film is allowed to remain remains in said the grooves and said unevenness to form a on the non-planar bottom portions as an interconnection layer.~~

12. (Amended) The manufacturing method of a semiconductor device according to claim 11, further comprising ~~the steps of~~:

forming a lower interconnection layer ~~as a lower layer~~ beneath said insulating layer; and

forming a connection hole for connecting said lower interconnection layer and said interconnection layer in said insulating layer, ~~wherein, prior to the formation of said forming the grooves, said and simultaneously forming the connection hole and said unevenness are simultaneously formed non-planar portions.~~

Amendments to the abstract:

ABSTRACT OF THE DISCLOSURE

~~A plurality of grooves~~ Grooves having different widths are formed ~~on in~~ a surface of an insulating film. ~~Interconnection constituted by~~ Interconnections including a barrier metal and a Cu film is formed ~~in a manner so as to be~~ are embedded in the respective grooves. ~~Unevenness formed by, for example, a plurality of grooves are formed on a~~ Uneven bottom portion of each of wide portions are formed in the wider grooves ~~having wide widths among the grooves~~. With this arrangement, it is possible to provide a semiconductor device and a manufacturing method thereof, which can reduce a difference in the deposition rate between the ~~wide wider~~ grooves and ~~narrow narrower~~ grooves.